140V High Efficiency Switching Surge Stopper

FEATURES

- **V_{OUT} Clamp Stops High Voltage Input Surges**
- **100% Duty Cycle Pass-Through Mode During Normal Operation**
- **Switches During Overvoltage or Overcurrent Transients and Faults and During Startup**
- **High Efficiency Switching Enables Long Duration Surge Protection and High Output Currents**
- **Wide V_{IN} Range: 4V to 140V (150V Abs Max)**
- **Adjustable Output Voltage Clamp Up to 60V**
- **Adjustable Output Overcurrent Protection**
- **R_{SENSE} or Inductor DCR Current Sensing**
- Power Inductor Reduces Input EMI in Normal Mode
- Adjustable Soft-Start for Inrush Current Limiting
- Programmable Fault Timer
- Open-Drain Fault Warning Indicator
- 2.7% Retry Duty Cycle During Faults
- Adjustable Switching Frequency: 50kHz to 900kHz
- Adjustable Input Voltage Turn-On Threshold
- Adjustable Input Overvoltage Lockout Threshold
- 20-Pin 4mm × 5mm QFN and TSSOP Packages

APPLICATIONS

- Automotive/Avionic/Industrial Surge Protection
- Automotive Load Dump Protection
- Vehicle Power Including ISO7637
- Military Power Including MIL1275

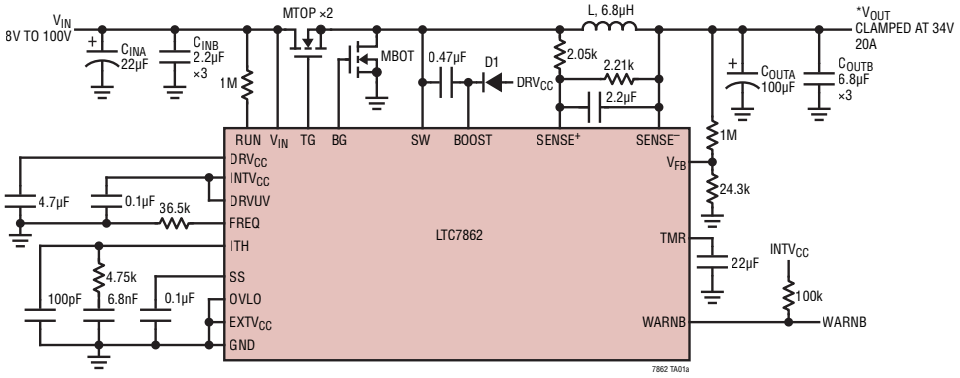
DESCRIPTION

The LTC®7862 high efficiency switching surge stopper protects loads from high voltage transients. High efficiency switching allows high output currents, small solution sizes, and high reliability. During an input overvoltage event, the LTC7862 controls the gates of two external N-channel MOSFETs to act as a switching DC/DC step-down regulator. This maintains the output voltage at a safe value, allowing the loads to continue to operate through the input overvoltage event. During normal operation, the LTC7862 turns on the top external N-channel MOSFET continuously, passing the input voltage through to the output, with minimal voltage drop. Using a fast peak current comparator, the LTC7862 also limits the maximum output current to protect against overcurrent and short-circuit faults.

An adjustable timer limits the time that the LTC7862 can spend switching during an overvoltage, overcurrent, or startup condition. When the timer expires, the external MOSFETs are turned off for a cooldown period and then the LTC7862 restarts. By strictly limiting how long the LTC7862 can switch, when the power loss is relatively high, the components and thermal design can be optimized for normal pass-through operation while still safely operating through high voltage input surges and/or overcurrent events.

TYPICAL APPLICATION

28V, 20A with 100V Overvoltage Protection

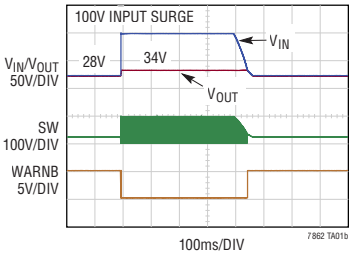


MTOP/MBOT: INFINEON BSC035N10NS5
L: COILCRAFT SER2918H-682KL
C_{INA}: SUNCON 160CE22LH
C_{INB}: TDK C4532X7R2A225K230KA

C_{OUTA}: SUN 63CE100LX
C_{OUTB}: TDK C4532X7R1H685K250KB
D1: NEXPERIA: PNE20010ER

* V_{OUT} FOLLOWS V_{IN} WHEN V_{IN} < 34V
V_{OUT} CLAMPS AT 34V WHEN V_{IN} > 34V

Overvoltage Protector Regulates Output at 28V During V_{IN} Transient

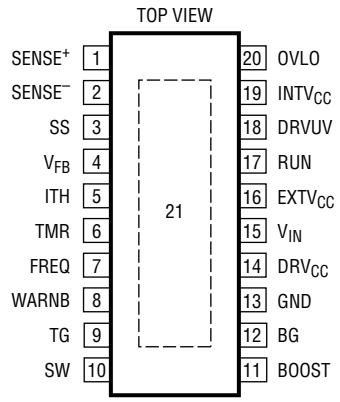


Rev 0

ABSOLUTE MAXIMUM RATINGS (Note 1)

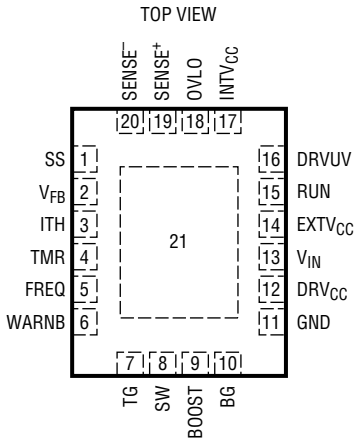
Input Supply Voltage (V_{IN}) ..... –0.3V to 150V
Top Side Driver Voltage BOOST ..... –0.3V to 150V
Switch Voltage (SW) ..... –5V to 150V
DRV_{CC}, (BOOST-SW) Voltages ..... –0.3V to 11V
BG, TG ..... (Note 8)
RUN Voltage ..... –0.3V to 150V
$SENSE^+$, $SENSE^-$ Voltages ..... –0.3V to 65V
FREQ, DRVUV Voltages ..... –0.3V to 6V
TMR, WARNB Voltages ..... –0.3V to 6V
$EXTV_{CC}$ Voltage ..... –0.3V to 14V
ITH, V_{FB} Voltages ..... –0.3V to 6V
SS, OVLO Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3)
LTC7862E, LTC7862I ..... –40°C to 125°C
LTC7862H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS

ORDER INFORMATION http://www.linear.com/product/LTC7862#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7862EFE#PBF	LTC7862EFE#TRPBF	LTC7862FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC7862IFE#PBF	LTC7862IFE#TRPBF	LTC7862FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC7862HFE#PBF	LTC7862HFE#TRPBF	LTC7862FE	20-Lead Plastic TSSOP	–40°C to 150°C
LTC7862EUFD#PBF	LTC7862EUFD#TRPBF	7862	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7862IUFD#PBF	LTC7862IUFD#TRPBF	7862	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7862HUFD#PBF	LTC7862HUFD#TRPBF	7862	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, V_{EXTVCC} = 0V, V_{DRVUV} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range	(Note 9) DRVUV = 0V	●	4		140	V
V_{OUT}	Regulated Output Clamp Voltage Set Point					60	V
V_{FB}	Regulated Feedback Voltage	(Note 4); ITH Voltage = 1.2V 0°C to 85°C ●	 ●	 0.792 0.788	 0.800 0.800	 0.808 0.812	 V V
I_{FB}	Feedback Current	(Note 4)			–0.006	±0.050	µA
	Feedback Voltage Line Regulation	(Note 4) V_{IN} = 4.5V to 150V			0.002	0.02	%/V
	Feedback Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 1.6V	●		–0.01	–0.1	%
g_m	Transconductance Amplifier gm	(Note 4) ITH = 1.2V, Sink/Source 5µA			2		mmho
I_Q	Input DC Supply Current	(Note 5) V_{FB} = 0.77V			1.2		mA
	Shutdown	RUN = 0V			10	20	µA
UVLO	Undervoltage Lockout	DRV_{CC} Ramping Up DRVUV = 0V DRVUV = $INTV_{CC}$	 ● ●	 	 4.0 7.5	 4.2 7.8	 V V
		DRV_{CC} Ramping Down DRVUV = 0V DRVUV = $INTV_{CC}$	 ● ●	 3.6 6.4	 3.8 6.7	 4.0 7.0	 V V
V_{RUN} ON	RUN Pin ON Threshold	V_{RUN} Rising	●	1.1	1.2	1.3	V
V_{RUN} Hyst	RUN Pin Hysteresis				80		mV
OVLO	Overvoltage Lockout Threshold	V_{OVLO} Rising	●	1.1	1.2	1.3	V
OVLO Hyst	OVLO Hysteresis				100		mV
	OVLO Delay				1		µs
	Feedback Overvoltage Protection	Measured at V_{FB}, Relative to Regulated V_{FB}		7	10	13	%
I_{SENSE}+	$SENSE^+$ Pin Current					±1	µA
I_{SENSE}–	$SENSE^–$ Pin Current	$SENSE^+$ = $SENSE^–$ = 28V			900		µA
	Maximum TG Duty Factor	In Dropout		100			%
I_{SS}	Soft-Start Charge Current	V_{SS} = 0V		8	10	12	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V, V_{SENSE}– = 28V	●	43	50	57	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, V_{EXTVCC} = 0V, V_{DRVUV} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver							
	TG Pull-up On-Resistance TG Pull-down On-Resistance	V_{DRVUV} = $INTV_{CC}$			2.2 1.0		Ω Ω
	BG Pull-up On-Resistance BG Pull-down On-Resistance	V_{DRVUV} = $INTV_{CC}$			2.0 1.0		Ω Ω
	TG Transition Time: Rise Time Fall Time	(Note 6) V_{DRVUV} = $INTV_{CC}$ C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	BG Transition Time: Rise Time Fall Time	(Note 6) V_{DRVUV} = $INTV_{CC}$ C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver, V_{DRVUV} = $INTV_{CC}$ (Note 6)			 55		 ns
	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver, V_{DRVUV} = $INTV_{CC}$ (Note 6)			 50		 ns
$t_{ON(MIN)}$	TG Minimum On-Time	(Note 7) V_{DRVUV} = $INTV_{CC}$			80		ns
Charge Pump for High Side Driver Supply							
I_{CPUMP}	Charge Pump Output Current	V_{BOOST} =16V, V_{SW} = 12V, V_{FREQ} = 0V V_{BOOST} =19V, V_{SW} = 12V, V_{FREQ} = 0V			65 55		µA µA
DRV_{CC} LDO Regulator							
	DRV_{CC} Voltage from V_{IN} LDO	V_{EXTVCC} = 0V 7V < V_{IN} < 150V, DRVUV = 0V 11V < V_{IN} < 150V, DRVUV = $INTV_{CC}$		 5.8 8.6	 6.0 9.0	 6.2 9.4	 V V
	DRV_{CC} Load Regulation from V_{IN} LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V DRVUV = 0V DRVUV = $INTV_{CC}$			 1.4 0.9	 2.5 2.0	 % %
	DRV_{CC} Voltage from $EXTV_{CC}$ LDO	7V < V_{EXTVCC} < 13V, DRVUV = 0V 11V < V_{EXTVCC} < 13V, DRVUV = $INTV_{CC}$		5.8 8.6	6.0 9.0	6.2 9.4	V V
	DRV_{CC} Load Regulation from $EXTV_{CC}$ LDO	I_{CC} = 0mA to 50mA DRVUV = 0V, V_{EXTVCC} = 8.5V DRVUV = $INTV_{CC}$, V_{EXTVCC} = 13V			 0.7 0.5	 2.0 2.0	 % %
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Ramping Positive DRVUV = 0V DRVUV = $INTV_{CC}$		 4.5 7.4	 4.7 7.7	 4.9 8.0	 V V
	$EXTV_{CC}$ Hysteresis				250		mV
$INTV_{CC}$ LDO Regulator							
V_{INTVCC}	$INTV_{CC}$ Voltage	I_{CC} = 0mA to 2mA		4.7	5.0	5.2	V
Oscillator and Phase-Locked Loop							
	Programmable Frequency	R_{FREQ} = 25k			105		kHz
	Programmable Frequency	R_{FREQ} = 65k		375	440	505	kHz
	Programmable Frequency	R_{FREQ} =105k			835		kHz
	Low Fixed Frequency	V_{FREQ} = 0V		320	350	380	kHz
	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$		485	535	585	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN} = 5V, V_{EXTVCC} = 0V, V_{DRVUV} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Fault Timer and WARNB Output							
$I_{SWITCHING}$	TMR Pull-Up Current (Switching)	TMR = 0V, V_{FB} = 0.83V	●	–35	–40	–45	µA
$I_{DROPOUT}$	TMR Pull-Down Current (Dropout)	TMR = 1V, V_{FB} = 0.77V	●	0.7	1.1	1.4	µA
$I_{COOLDOWN}$	TMR Pull-Down Current (Cool-Down)	TMR = 2.5V	●	0.7	1.1	1.4	µA
	TMR Switching Off Threshold		●	2.13	2.19	2.23	V
	TMR Retry Threshold			0.19	0.25	0.31	V
	TMR Switching Set Time (Initial Fault Period) per 1µF			52	55	58	ms/µF
	TMR Switching Set Time (Retry Period) per 1µF				50		ms/µF
	TMR Cool-Down Time per 1µF				1700		ms/µF
D_{RETRY}	Retry Duty Cycle During a Sustained Fault			1.8	2.7	3.5	%
V_{WARNB}	WARNB Voltage Low	I_{WARNB} = 2mA			0.02	0.04	V
I_{WARNB}	WARNB Leakage Current	V_{WARNB} = 3.3V				10	µA
t_{WARNB}	Delay from TG Going High to WARNB Going High Impedance				60		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC7862 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7862E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7862I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC7862H is guaranteed over the –40°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 38°C/W for the TSSOP package and θ_{JA} = 43°C/W for the QFN package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC7862 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC7862E and LTC7862I, 150°C for the LTC7862H). For the LTC7862I and LTC7862H, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at –40°C.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

Note 8: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

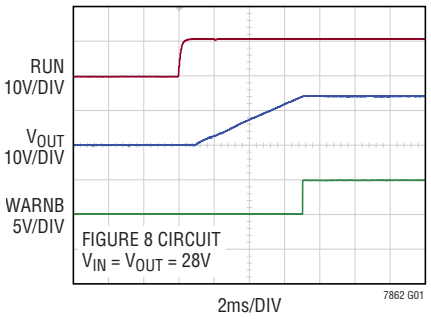
Note 9: The minimum input supply operating range is dependent on the DRV_{CC} UVLO thresholds as determined by the DRVUV pin setting.

Note 10: All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

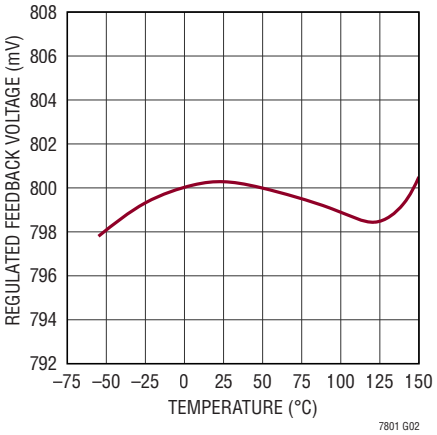
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

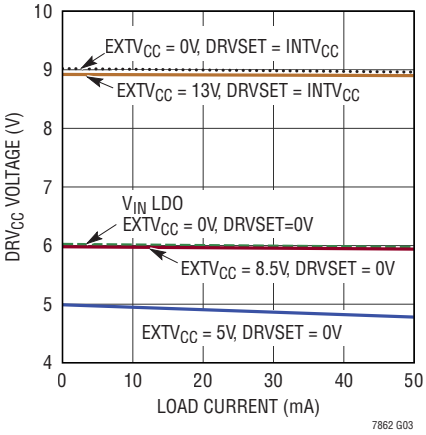
Soft Start-Up



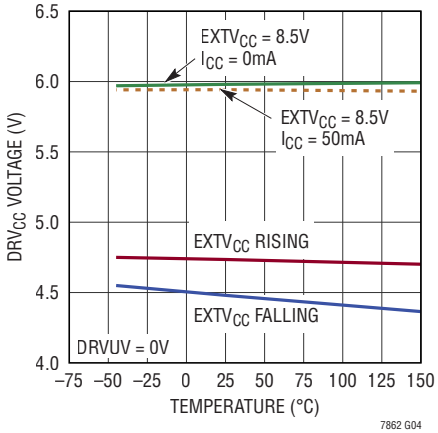
Regulated Feedback Voltage vs Temperature



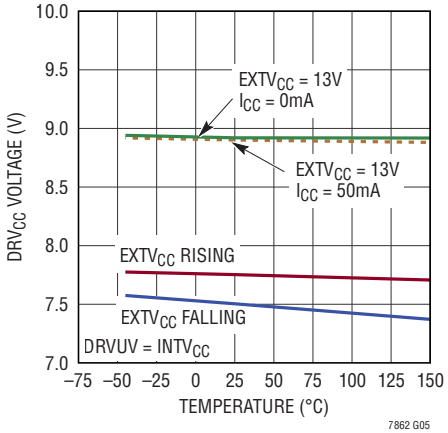
DRVCC and EXTVCC vs Load Current



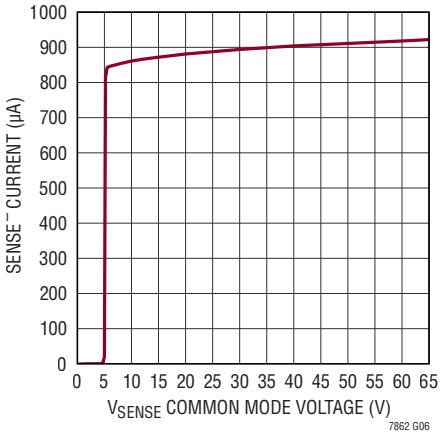
EXTVCC Switchover and DRVCC Voltages vs Temperature



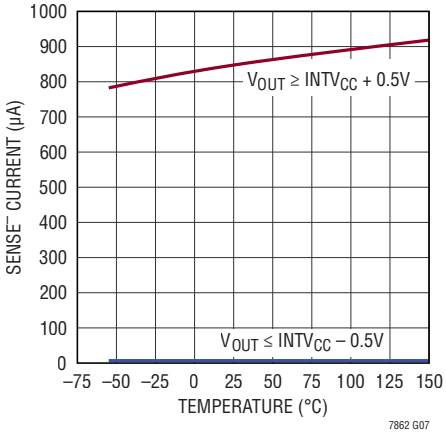
EXTVCC Switchover and DRVCC Voltages vs Temperature



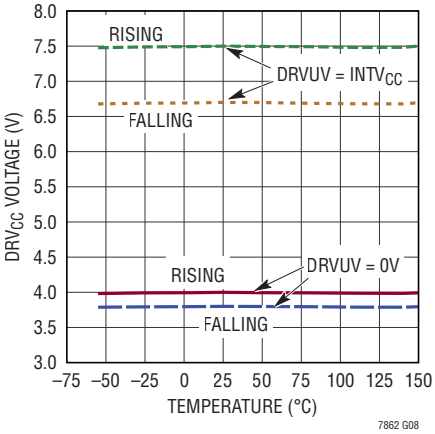
SENSE– Pin Input Current vs VSENSE Voltage



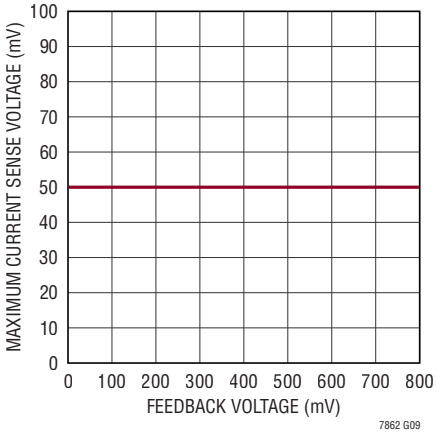
SENSE– Pin Input Bias Current vs Temperature



Undervoltage Lockout Threshold vs Temperature



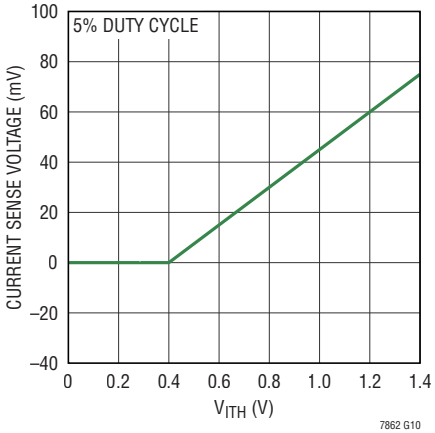
Current Limit vs Feedback Voltage



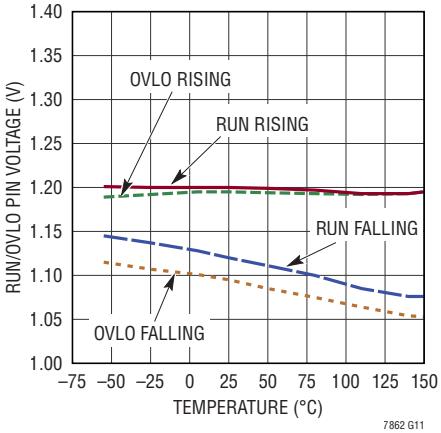
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

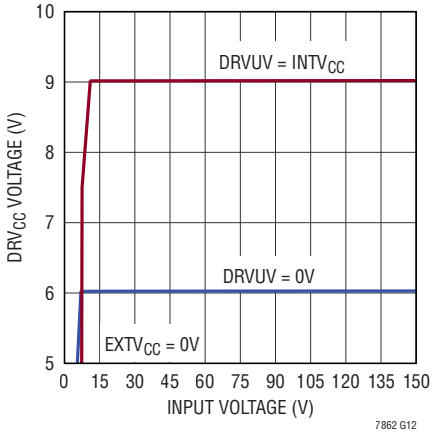
Maximum Current Sense Threshold vs ITH Voltage



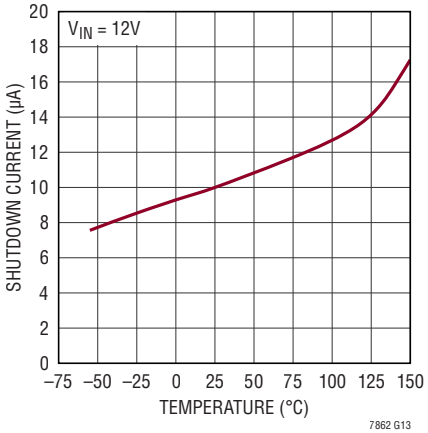
RUN/OVLO Threshold vs Temperature



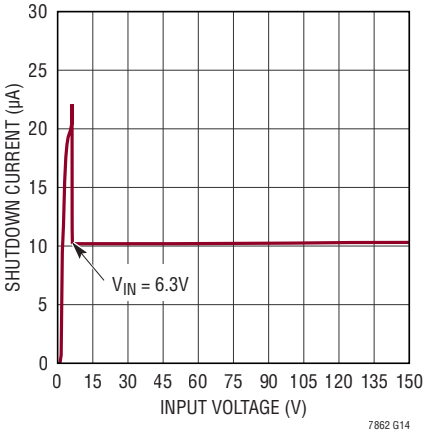
DRV_{CC} Line Regulation



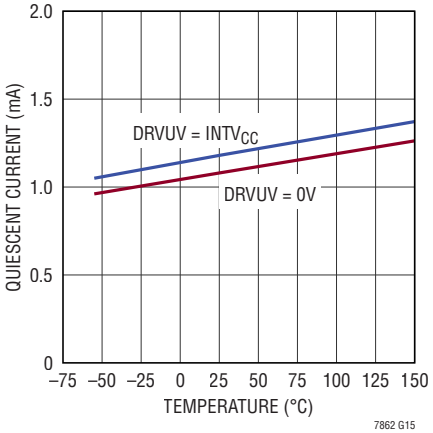
Shutdown Current vs Temperature



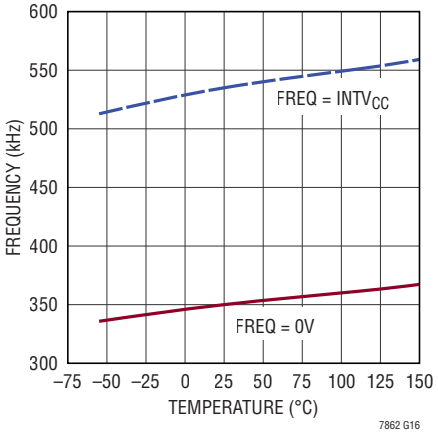
Shutdown Current vs Input Voltage



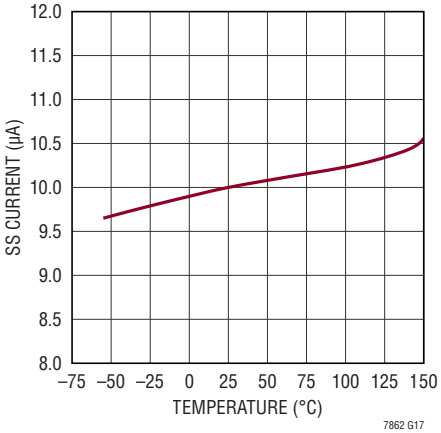
Quiescent Current vs Temperature



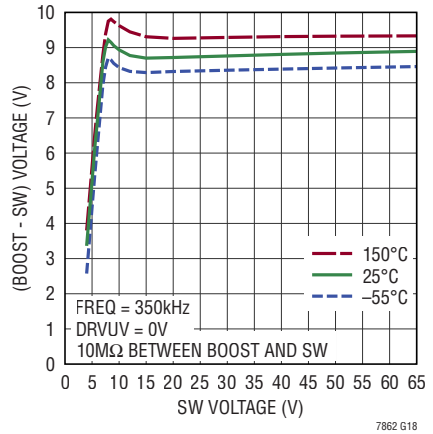
Oscillator Frequency vs Temperature



SS Pull-Up Current vs Temperature



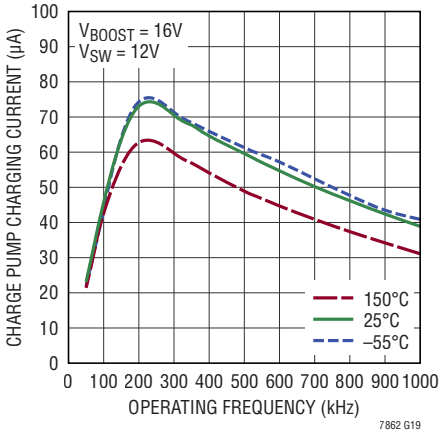
Boost Charge Pump Voltage vs SW Voltage in Pass-Through Mode



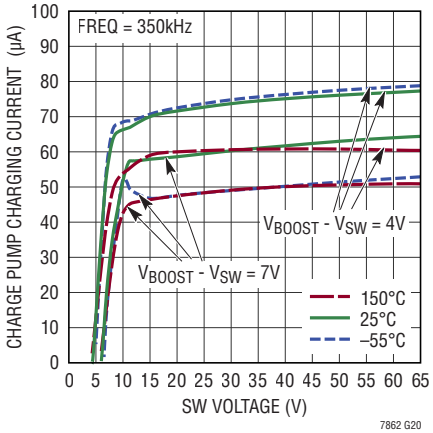
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

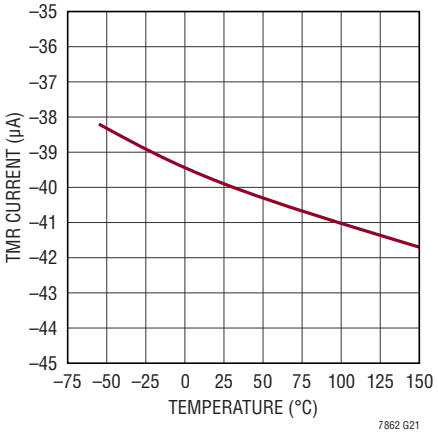
BOOST Charge Pump Charging Current vs Frequency



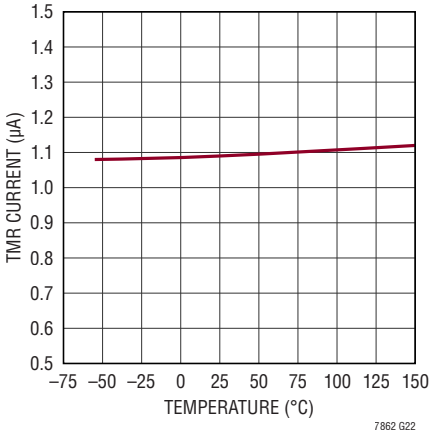
BOOST Charge Pump Charging Current vs SW Voltage



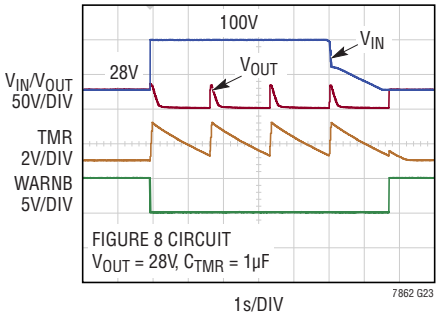
TMR Pull-Up Current vs Temperature



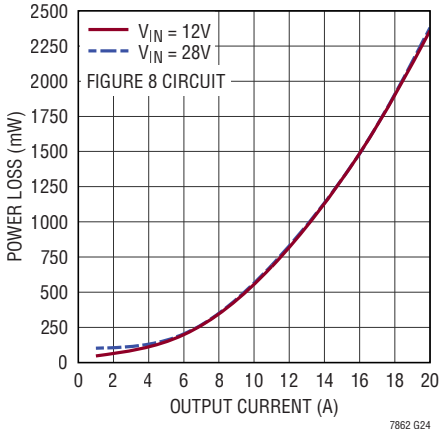
TMR Pull-Down Current vs Temperature



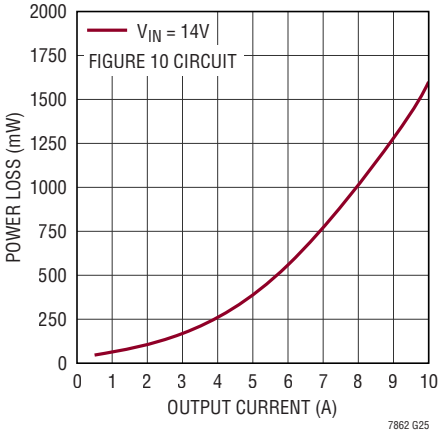
Sustained Overvoltage Fault



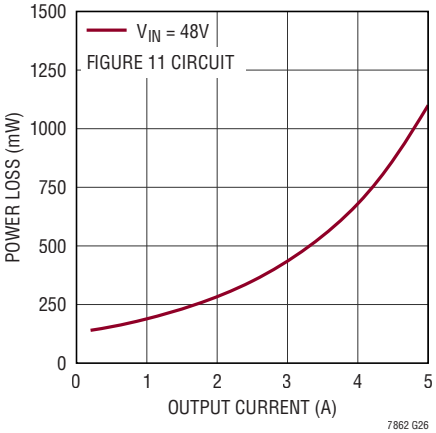
Power Loss vs Output Current in Pass-Through Mode



Power Loss vs Output Current in Pass-Through Mode



Power Loss vs Output Current in Pass-Through Mode



PIN FUNCTIONS (QFN/TSSOP)

SS (Pin 1/Pin 3): Soft-Start Input. The LTC7862 attempts to regulate the V_{FB} voltage to the smaller of 0.8V or the voltage on the SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage during startup or during a retry.

V_{FB} (Pin 2/Pin 4): Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistor divider across the output.

ITH (Pin 3/Pin 5): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

TMR (Pin 4/Pin 6): Programmable Fault Timer Input. A timing capacitor C_{TMR}, connected between this pin and GND, sets the amount of time that can be spent switching (during an overvoltage, overcurrent, and/or startup condition.) It also sets the cool-down time before the LTC7862 will retry. See Applications Information.

FREQ (Pin 5/Pin 7): Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed by using a resistor between FREQ and GND. An internal 20µA pull-up current develops the voltage to be used by the VCO to control the frequency.

WARNB (Pin 6/Pin 8): Open-Drain Logic Output. This pin pulls low to GND whenever the LTC7862 is switching (during an overvoltage, overcurrent, and/or startup condition.) The typical pull-down impedance is 10Ω. The WARNB pin enters a high-impedance state 60µs after LTC7862 enters dropout with the top external MOSFET on continuously. The WARNB pin is also pulled low during shutdown and during the cool-down period before a retry.

TG (Pin 7/Pin 9): High Current Gate Drive for Top N-Channel MOSFET. This is the output of the floating high side driver with a voltage swing from SW to BOOST.

SW (Pin 8/Pin 10): Switch Node Connection to Inductor.

BOOST (Pin 9/Pin 11): Bootstrapped Supply to the Topside Floating Driver. A capacitor is connected between the BOOST and SW pins and an external low leakage diode is tied between the BOOST and DRV_{CC} pins. Voltage swing at the BOOST pin is from approximately DRV_{CC} to (V_{IN} + DRV_{CC}). When TG is statically on during normal operation, BOOST is approximately 9V above SW.

BG (Pin 10/Pin 12): High Current Gate Drive for Bottom (Synchronous) N-Channel MOSFET. Voltage swing at this pin is from ground to DRV_{CC}.

GND (Pin 11, Exposed Pin 21/Pin 13, Exposed Pad Pin 21): Ground. All GND pins must be tied together for operation. The exposed pad must be soldered to PCB ground for rated electrical and thermal performance.

DRV_{CC} (Pin 12/Pin 14): Output of the V_{IN} or $EXTV_{CC}$ Low Dropout Regulators. The gate drivers are powered from this voltage source. The DRV_{CC} voltage is set by the DRVUV pin. Must be decoupled to ground with a minimum of 4.7µF ceramic or other low ESR capacitor, as close as possible to the IC. Do not use the DRV_{CC} pin for any other purpose.

V_{IN} (Pin 13/Pin 15): Main Supply Pin. A bypass capacitor should be tied between this pin and GND.

$EXTV_{CC}$ (Pin 14/Pin 16): External Power Input to an Internal LDO linear regulator Connected to DRV_{CC}. This LDO supplies DRV_{CC} power from $EXTV_{CC}$, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than its switchover threshold (4.7V or 7.7V depending on the DRVUV pin). See DRV_{CC} Regulators in the Applications Information section. Do not exceed 14V on this pin. Do not connect $EXTV_{CC}$ to a voltage greater than V_{IN}.

RUN (Pin 15/Pin 17): Run Control Input. Forcing this pin below 1.12V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC7862, reducing quiescent current to approximately 10µA. This pin can be tied to V_{IN} for always-on operation. Do not float this pin.

PIN FUNCTIONS (QFN/TSSOP)

DRVUV (Pin 16/Pin 18): DRV_{CC} Regulation and UVLO Program Pin. This pin sets the regulated output voltage of the DRV_{CC} linear regulator. Tying this pin to GND sets DRV_{CC} to 6.0V. Tying this pin to $INTV_{CC}$ sets DRV_{CC} to 9V. This pin also determines the higher or lower DRV_{CC} UVLO and $EXTV_{CC}$ switchover thresholds, as listed on the Electrical Characteristics table. Connecting DRVUV to GND chooses the lower thresholds whereas tying DRVUV to $INTV_{CC}$ chooses the higher thresholds. Do not float this pin.

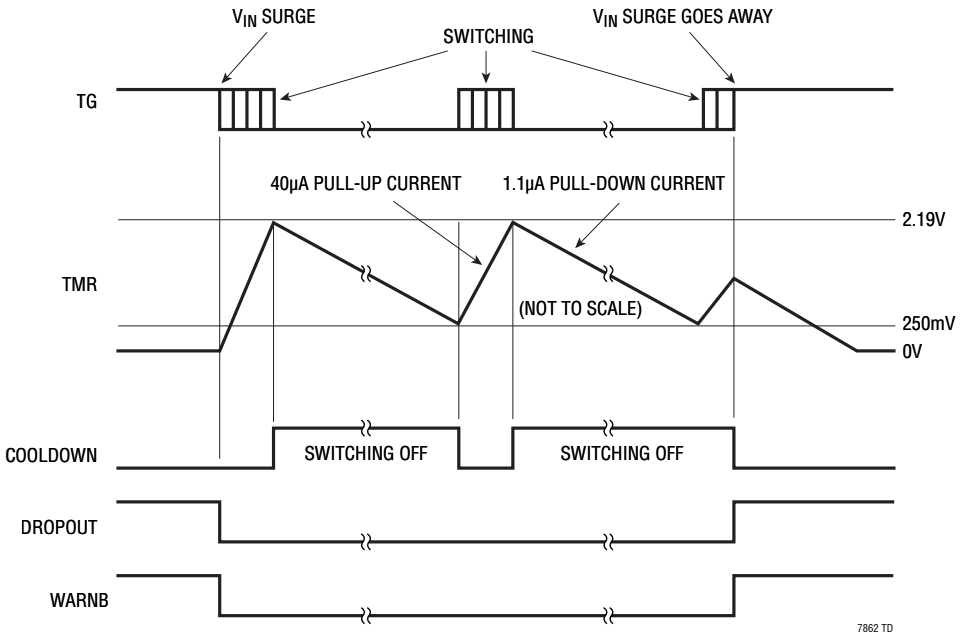
$INTV_{CC}$ (Pin 17/Pin 19): Output of the Internal 5V Low Dropout Regulator. Many of the low voltage analog and digital circuits are powered from this voltage source. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the LTC7862.

OVLO (Pin 18/Pin 20): Overvoltage Lockout Input. A voltage on this pin above 1.2V disables switching of the controller. The DRV_{CC} and $INTV_{CC}$ supplies maintain regulation during an OVLO event. Exceeding the OVLO threshold triggers a soft-start reset. If the OVLO function is not used, connect this pin to GND.

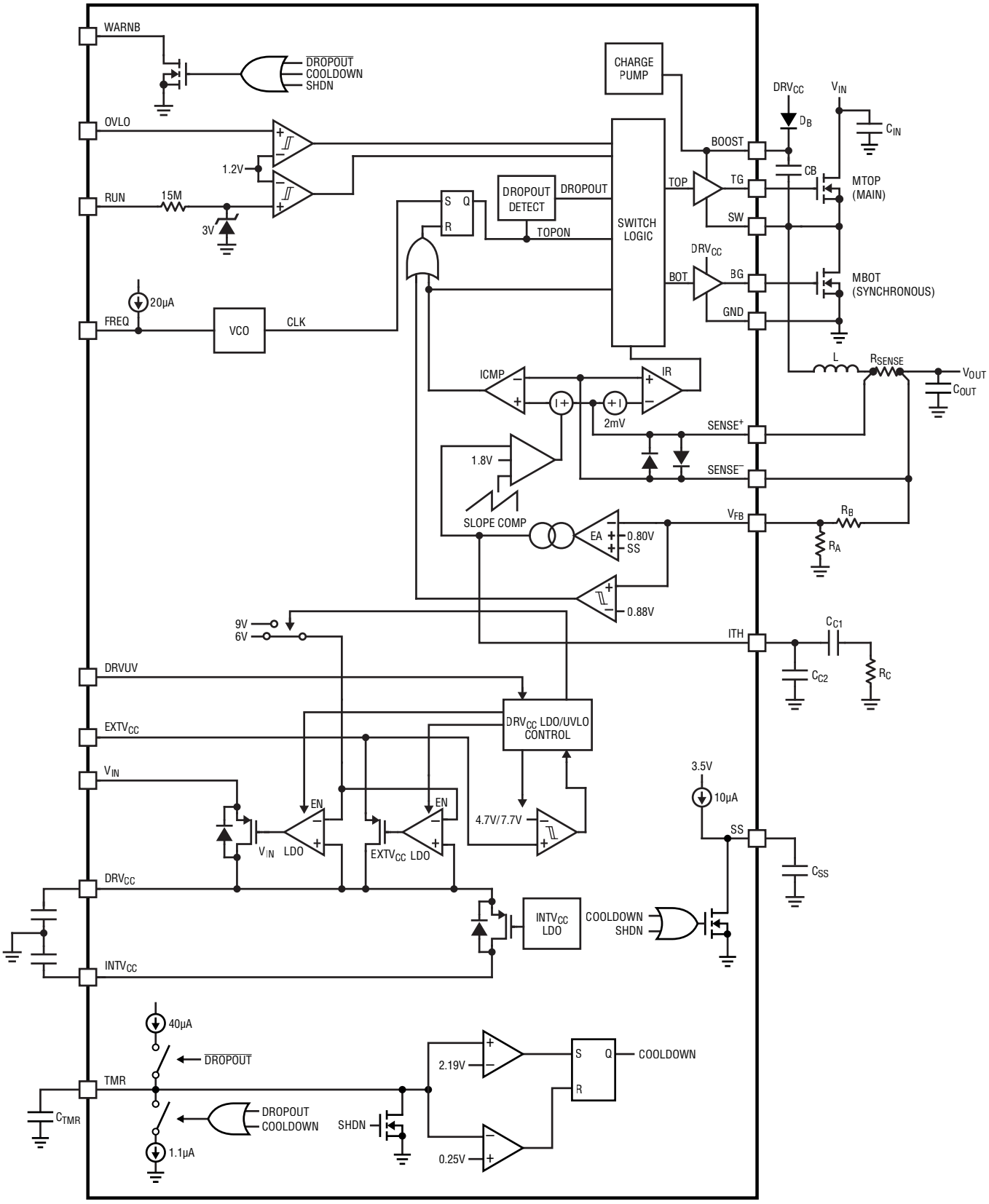
$SENSE^+$ (Pin 19/Pin 1): The (+) Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

$SENSE^-$ (Pin 20/Pin 2): The (–) Input to the Differential Current Comparator. When $SENSE^-$ is greater than $INTV_{CC}$, the $SENSE^-$ pin supplies power to the current comparator.

TIMING DIAGRAM



FUNCTIONAL DIAGRAM



OPERATION

High Efficiency Switching Surge Stopper Overview

The LTC7862 is a high efficiency switching surge stopper controller. “Normal” operation for the LTC7862 is in “dropout” mode, in which the top external N-channel MOSFET is turned on continuously (100% duty cycle) passing the input voltage through to the output with minimal voltage drop. During an input overvoltage event, the LTC7862 switches the gates of the top and bottom N-channel MOSFETs to act as a switching DC/DC step-down regulator. This maintains the output voltage at a safe, user-programmed clamp voltage level. Similarly, the LTC7862 switches in response to an overcurrent or short-circuit event. The LTC7862 also switches during startup to limit inrush current and to smoothly ramp the output voltage. If the time spent during any of these switching events exceeds the time programmed by the fault timer pin (TMR), the LTC7862 will cease switching for a cool-down period and then attempt to restart.

An LTC7862 high efficiency switching surge stopper can be thought of as a pre-regulator. Consider as an example a MIL1275 application, where the input voltage connects to a nominal 28V vehicle power bus. The power bus can drop as low as 12V during engine cranking, and can also surge up to 100V with a total surge duration lasting up to 500ms. A switching surge stopper can be placed between the input power bus and any downstream load to protect the load from potentially destructive voltage levels. The output voltage of the switching surge stopper is pre-regulated or clamped to a safe voltage, such as 34V. Whenever the input voltage is above 34V, the LTC7862 switches and limits the output voltage to 34V. Whenever the input voltage is less than 34V, the LTC7862 is in normal mode and passes the input voltage through to the output with no switching.

For both a traditional linear regulator surge stopper (such as LTC4363) and the LTC7862 high efficiency switching surge stopper, the power loss increases significantly during the input voltage surge when regulation begins. In a linear regulator surge stopper, the power loss is simply the output current times the difference between the input and output voltages, which can be very large. In a switching surge stopper, the power loss is determined by the switching regulator’s conversion efficiency, which is relatively high. This enables the LTC7862 high efficiency switching surge stopper to deliver much higher output current and power levels compared to a traditional linear regulator surge stopper.

Furthermore, by using the LTC7862’s timer, the time spent switching in regulation can be limited, allowing the operating power to be pushed beyond what could otherwise be achieved if the switching regulator were required to run continuously in steady-state. The use of the timer improves reliability and reduces component size compared to a continuous solution. The timer also allows the external components to be optimized for the normal pass-through mode in which the switching surge stopper spends the vast majority of its operating life. In this normal mode, the switching surge stopper is effectively acting as a wire with a conduction power loss (sometimes referred to as an insertion loss) equal to the output current times the sum of the resistances of the top MOSFET, inductor, and current sense resistor.

In particular, a relatively low $R_{DS(ON)}$ (with typically high gate charge) top MOSFET can be selected. This reduces power loss in normal operation, but significantly increases the power loss when switching due to transition losses in the top MOSFET. Usually, in traditional high input voltage switching step-down regulators, a low gate charge (with typically high $R_{DS(ON)}$) top MOSFET is desired to minimize transition power losses. But since the LTC7862’s timer limits the time spent switching, this increased power loss can be safely tolerated. Likewise, the inductor value and switching frequency can be chosen to minimize the insertion loss at the expense of switching losses. This allows the LTC7862 switching surge stopper to operate at a higher switching frequency than what would be feasible in a continuous solution without a timer. This results in a physically smaller inductor with a lower inductance and lower DC resistance.

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Main Control Loop

The LTC7862 uses a constant frequency, peak current mode step-down architecture. During switching operation, the external top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$DRV_{CC}/EXTV_{CC}/INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed to 6V or 9V using the DRVUV pin. Two separate LDOs (low dropout linear regulators) can provide power from V_{IN} to DRV_{CC}. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins.

When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVUV pin), the V_{IN} LDO is enabled and supplies power from V_{IN} to DRV_{CC}.

If $EXTV_{CC}$ is taken above its switchover voltage, the V_{IN} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power from $EXTV_{CC}$ to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source such as one derived from the LTC7862 switching regulator output.

The $INTV_{CC}$ supply powers most of the other internal circuits in the LTC7862. The $INTV_{CC}$ LDO regulates to a fixed value of 5V and its power is derived from the DRV_{CC} supply.

Top MOSFET Driver, Charge Pump and Pass-Through Mode

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which recharges during each switching cycle through an external diode, D_B, whenever SW goes low.

If the input voltage is below the regulated output (clamp) voltage, the loop enters dropout and turns on the top MOSFET continuously. The LTC7862 includes an internal charge pump that allows the top MOSFET to be turned on continuously at 100% duty cycle. This charge pump delivers current to C_B to keep it biased at approximately 8.5V.

Shutdown and Start-Up (RUN, SS Pins)

The LTC7862 can be shut down using the RUN pin. Connecting the RUN pin below 1.12V shuts down the main control loop. Connecting the RUN pin below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this state, the LTC7862 draws only 10µA of quiescent current.

The RUN pin has no internal pull-up current, so the pin must be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down.

The start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference, the LTC7862 regulates the V_{FB} voltage to the SS pin voltage instead of the 0.8V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to GND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 0.8V (and

OPERATION

beyond), the output voltage V_{OUT} rises smoothly from zero to its final value.

Light Load Current Operation (Pulse-Skipping Mode)

In switching mode, LTC7862 enters constant frequency pulse-skipping mode at light load currents.

In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation).

Frequency Selection (FREQ Pin)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC7862 can be selected using the FREQ pin.

The FREQ pin can be tied to GND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 1.

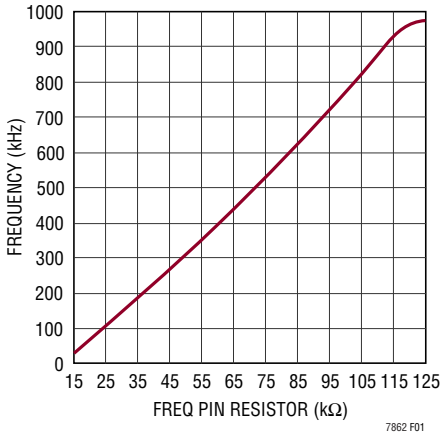


Figure 1. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Table 1 summarizes the different states in which the FREQ pin can be used.

Table 1.

FREQ PIN	FREQUENCY
0V	350kHz
$INTV_{CC}$	535kHz
Resistor to GND	50kHz to 900kHz

Input Supply Overvoltage Lockout (OVLO Pin)

The LTC7862 implements a protection feature that stops all switching and turns off both the top and bottom external MOSFETs when the input voltage rises above a programmable operating range. By using a resistor divider from the input supply to ground, the OVLO pin serves as a precise input supply voltage monitor. Switching is disabled when the OVLO pin rises above 1.2V, which can be configured to limit switching to a specific range of input supply voltage.

When switching is disabled, the LTC7862 can safely sustain input voltages up to the absolute maximum rating of 150V. Input supply overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7862 application circuit. LTC7862 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, a current sensing resistor provides the most accurate current limit for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparator. The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC7862 to regulate an output clamp voltage up to a nominal set point of 60V (allowing margin for tolerances and transients). The SENSE+ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the SENSE– pin changes depending on the common mode voltage. When SENSE– is less than $INTV_{CC}$ – 0.5V, it is high impedance, drawing less than ≈1µA. When SENSE– is above $INTV_{CC}$ + 0.5V, a higher current (≈900µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

Filter components mutual to the sense lines should be placed close to the LTC7862, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 2). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 3b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

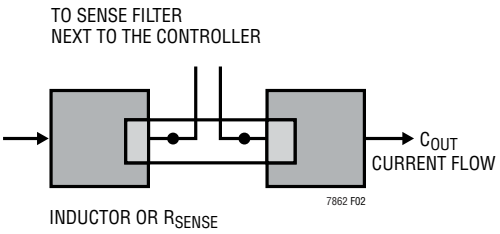


Figure 2. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

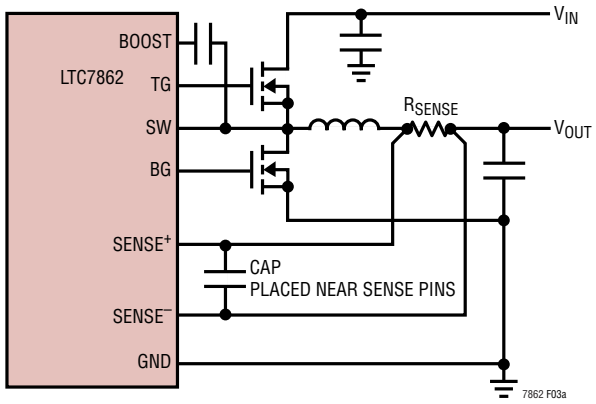
A typical sensing circuit using a discrete resistor is shown in Figure 3a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ = 50mV typical. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

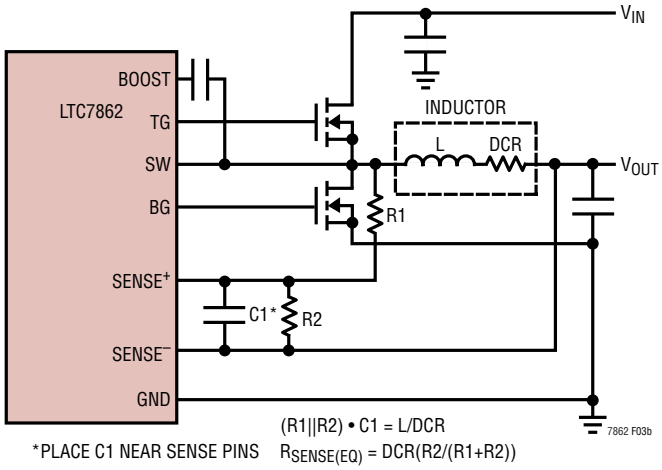
$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Normally in high duty cycle conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion operating at greater than 50% duty factor. The LTC7862, however, uses a proprietary circuit to nullify the effect of slope compensation on the current limit performance.

APPLICATIONS INFORMATION



(3a) Using a Resistor to Sense Current



(3b) Using the Inductor DCR to Sense Current

Figure 3. Current Sensing Methods

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7862 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency and higher power loss compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

APPLICATIONS INFORMATION

The values for R1 and R2 are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\,R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

APPLICATIONS INFORMATION

Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC7862 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can be 6V or 9V depending on configuration of the DRVUV pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

Selection criteria for the power MOSFET for normal pass-through operation include the on-resistance $R_{DS(ON)}$, input voltage and maximum output current.

The MOSFET power dissipation at maximum output current are given by:

$P_{MAIN} = (I_{OUT(MAX)})^2 (1+ \delta)R_{DS(ON)}$

P_{SYNC} = 0 (Synchronous FET is OFF during normal pass-through operation)

where δ is the temperature dependency of $R_{DS(ON)}$. The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

Selection criteria for the power MOSFETs during timer-enabled switching operation include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is switching in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} +$$

$$(V_{IN})^2\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER})\bullet$$

$$\left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The MOSFET's temperature rise due to power dissipation must be considered. Refer to Thermal Considerations section for more details.

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation (1) to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2} \quad (1)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7862, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC7862, is also suggested. A small (≤10Ω) resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting Output Clamp Voltage

The LTC7862 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 4. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

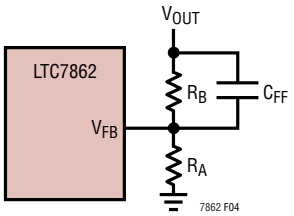


Figure 4. Setting Output Voltage

RUN Pin and Overvoltage/Undervoltage Lockout

The LTC7862 is enabled using the RUN pin. It has a rising threshold of 1.2V with 80mV of hysteresis. Pulling the RUN pin below 1.12V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this state the LTC7862 draws only 10µA of quiescent current.

The RUN pin is high impedance below 3V and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down. Above 3V, the RUN pin has approximately a 15MΩ impedance to an internal 3V clamp.

APPLICATIONS INFORMATION

The RUN and OVLO pins can alternatively be configured as undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistor divider from V_{IN} to ground. A simple resistor divider can be used as shown in Figure 5 to meet specific V_{IN} voltage requirements.

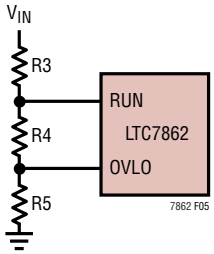


Figure 5. Adjustable UV and OV Lockout

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC7862, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megaohm range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R3+ R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}.

The individual values of R3, R4 and R5 can be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.20V}{\text{RISING } V_{IN} \text{ OVLO THRESHOLD}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.20V}{\text{RISING } V_{IN} \text{ RUN THRESHOLD}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not require a precise OVLO, the OVLO pin can be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with R5 = 0Ω.

Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal DRV_{CC} UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω.

Soft-Start (SS) Pin

The start-up of V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 0.8V reference, the LTC7862 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of the internal reference. The SS pin can be used to program an external soft-start function.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 6. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC7862 will regulate its feedback voltage (and hence V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

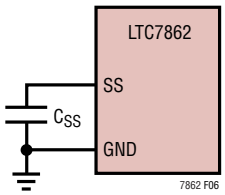


Figure 6. Using the SS Pin to Program Soft-Start

APPLICATIONS INFORMATION

DRV_{CC} Regulators

The LTC7862 features two separate low dropout linear regulators (LDO) that can supply power at the DRV_{CC} pin. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. The internal $EXTV_{CC}$ LDO uses an internal P-channel pass device between the $EXTV_{CC}$ and DRV_{CC} pins.

The DRV_{CC} supply is regulated to 6V or 9V, depending on how the DRVUV pin is set. The internal V_{IN} and $EXTV_{CC}$ LDOs can supply a peak current of at least 50mA. The DRV_{CC} pin must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

The DRVUV pin programs the DRV_{CC} supply voltage and also selects different DRV_{CC} UVLO and $EXTV_{CC}$ switchover threshold voltages. Tables 2a and 2b summarize the different DRVUV pin configurations along with the voltage settings that go with each configuration. Tying the DRVUV pin to $INTV_{CC}$ programs DRV_{CC} to 9V. Tying the DRVUV pin to GND programs DRV_{CC} to 6V.

Table 2a.

DRVUV PIN	DRV_{CC} VOLTAGE
GND	6V
$INTV_{CC}$	9V

Table 2b.

DRVUV	DRV_{CC} UVLO RISING/FALLING THRESHOLDS	$EXTV_{CC}$ SWITCHOVER RISING/FALLING THRESHOLD
GND	4.0V/3.8V	4.7V/4.45V
$INTV_{CC}$	7.5V/6.7V	7.7V/7.45V

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7862 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by the V_{IN} LDO, or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V or 7.7V as determined by the DRVUV pin described above), the V_{IN} LDO is enabled. Power dissipation in this case is highest and is equal to $V_{IN} \bullet I_{DRVCC}$ and is dissipated inside the IC. The gate charge current is dependent on operating frequency.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVUV pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 14V, DRV_{CC} is regulated to the programmed voltage.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from the LTC7862's switching regulator output ($4.7V/7.7V \le V_{OUT} \le 14V$). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and DRV_{CC} pins. In this case, do not apply more than 10V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \le V_{IN}$.

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The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause DRV_{CC} to be powered from the internal V_{IN} LDO.
2. $EXTV_{CC}$ connected directly to the regulator output from 5V to 14V.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC} \leq V_{IN}$.
4. $EXTV_{CC}$ connected to the regulator output through an external zener diode. If the output voltage is greater than 14V, a zener diode can be used to drop the necessary voltage between V_{OUT} and $EXTV_{CC}$ such that $EXTV_{CC}$ remains below 14V (Figure 7). In this configuration, a bypass capacitor on $EXTV_{CC}$ of at least 0.1µF is recommended. An optional resistor between $EXTV_{CC}$ and GND can be inserted to ensure adequate bias current through the Zener diode.

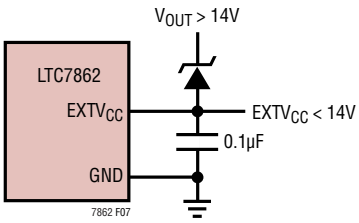

Figure 7. Using a Zener Diode Between V_{OUT} and $EXTV_{CC}$

$INTV_{CC}$ Regulator

An additional P-channel LDO supplies power at the $INTV_{CC}$ pin from the DRV_{CC} pin. Whereas DRV_{CC} powers the gate drivers, $INTV_{CC}$ powers much of the LTC7862's internal circuitry. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor. $INTV_{CC}$ is also used as a pull-up to bias other pins, such as FREQ and WARNB.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged through the external low leakage diode, D_B, from DRV_{CC} when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the BOOST voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

External BOOST Diode Selection (D_B)

A Schottky diode should not be used between DRV_{CC} and BOOST, as the reverse leakage of the Schottky diode at hot will be more current than the charge pump can provide.

Some example of silicon diodes with low leakage include:

CMHD3595, CMDD3003: Central Semiconductor

ES1DR, PNE20010ER: Nexperia

Fault Conditions: Current Limit

Under short-circuit conditions with very low duty cycles, the LTC7862 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC7862 (≈80ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)}$$

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Fault Conditions: Output Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator detects faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on chip, the overtemperature shutdown circuitry will shut down the LTC7862. When the junction temperature exceeds approximately 175°C, the overtemperature circuitry disables the DRV_{CC} LDO, causing the DRV_{CC} supply to collapse and effectively shutting down the entire LTC7862 chip. Once the junction temperature drops back to the approximately 155°C, the DRV_{CC} LDO turns back on. Long term overstress (T_J > 150°C) should be avoided as it can degrade the performance or shorten the life of the part.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC7862 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC7862 is approximately 80ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 130ns. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

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Thermal Considerations

The sustained or static power loss in normal pass-through operation must be limited to ensure suitable maximum component temperatures during all normal operating conditions. The temperature rise of a switching surge stopper is best measured empirically. Power loss for the pass-through power path is I^2R_{SW-ON} and may be calculated according to the equation below.

$$I^2R_{SW-ON} = I^2 \bullet (R_{SENSE} + R_{DS(ON)(TOPMOSFET)} + R_{INDUCTOR})$$

The dynamic or transient power loss during switching operation is of concern with respect to component temperature rise and is principally managed by the timer function which sets a maximum time in this mode. Thermal mass and thermal resistance play key roles in determining the peak temperatures of components at the point in time when the timer cycles off and shuts down.

Worst-case operation for a single fault shorted output is typically with the input voltage in the high normal operating range and the output shorted. For this condition, the bottom synchronous MOSFET is typically the hottest component, as it conducts nearly all the peak current at a high duty cycle. Worst-case operation for a single fault input voltage surge is with the input at the maximum expected input voltage and the maximum operational load current. An input voltage surge and output short is a double fault and may not be required. Specific fault testing and design margin is determined by system requirements.

Thermal evaluation and timer setting can be most easily done empirically by observing key component temperatures dynamically in various fault conditions. Observe peak temperatures with an instrument with sufficient bandwidth to track temperatures, such as an infrared (IR) camera. One with video capability is ideal.

Set a maximum temperature rise goal based on component maximum junction temperature ratings, maximum expected ambient temperature, and allowed junction to case temperature rise. Start at lower input voltages and/or longer TMR timer settings and change after empirical system verification and measurement.

Fault Timer (TMR)

The LTC7862 is a switching surge stopper. The LTC7862 switches only during startup, during an overcurrent fault, and/or during an input overvoltage surge. The primary function of a switching surge stopper is to limit the output to a programmed maximum voltage during an input voltage surge. Limiting the output voltage "surge stops" the input voltage surge and prevents it from propagating to the system and potentially causing damage.

The switching surge stopper external components are typically optimized to minimize the total resistance in normal (dropout) operation when the top MOSFET is on continuously. The LTC7862's fault timer is used to limit the time spent switching. The fault timer is programmed to allow the switching surge stopper components to operate within a safe temperature range with the increased power losses incurred during switching. Since the LTC7862 timer may stop switching before reaching thermal equilibrium, the power rating can be significantly increased compared to what could be achieved without a timer. Likewise, for a given output power rating, a smaller, cooler, and less costly solution can be achieved by using the timer.

Connecting a capacitor from the TMR pin to ground sets the amount of time that the LTC7862 is allowed to switch. This same capacitor also sets a cooldown period before the LTC7862 is allowed to switch again. During normal operation, a 1.1µA current source pulls down on the TMR pin. While the LTC7862 is switching, a 40µA current source pulls up on the TMR pin. If the TMR pin is charged up to 2.19V, the LTC7862 stops switching with both external MOSFETs held off (TG and BG held low). This limits the switching time to:

$$T_{SWITCHING} = 2.19V \bullet C_{TMR}/40\mu A$$

If the LTC7862 returns to normal operation before the timer reaches 2.19V, the 1.1µA pull-down current source discharges TMR, and the LTC7862 is allowed to switch immediately if conditions warrant.

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If the timer reaches 2.19V, the LTC7862 is not allowed to switch again until TMR is discharged down to 0.25V by a 1.1µA current source. This sets a time period that permits the switching surge stopper components to cool down before attempting to switch again. This cooldown period is given by:

$$T_{COOLDOWN} = (2.19V – 0.25V) • C_{TMR}/1.1µA$$

After this cooldown period, the LTC7862 may try to switch again. On this retry, the time spent switching is limited to

$$T_{RETRY} = 1.94V • C_{TMR}/40µA$$

During a sustained fault condition, this results in a retry duty cycle that is to first order independent of C_{TMR} and is defined by:

$$D = 100 • T_{RETRY}/(T_{COOLDOWN} + T_{RETRY}) = 100 • 1/36.4 \approx 2.7\%$$

Warning Indicator (WARNB)

The WARNB pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the WARNB pin low to ground (GND) whenever the LTC7862 is switching (i.e, not in dropout) during an overvoltage or overcurrent fault or during startup. The WARNB pin is also pulled low during shutdown and during the cooldown period after a fault timeout. The MOSFET is turned off and the WARNB pin enters a high-impedance state 60µs after the LTC7862 enters normal operation (dropout) with the top external MOSFET (TG) on continuously. The WARNB pin is normally pulled up by an external resistor to a voltage source no greater than 6V.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the first page circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

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A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{DRVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, bottom N-channel MOSFET and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other.
2. Does the LTC7862 V_{FB} pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
3. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
4. Is the DRV_{CC} and decoupling capacitor connected close to the IC, between the DRV_{CC} and the ground pin? This capacitor carries the MOSFET drivers' current peaks.
5. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC7862 and occupy minimum PC trace area.
6. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the output to verify operation.

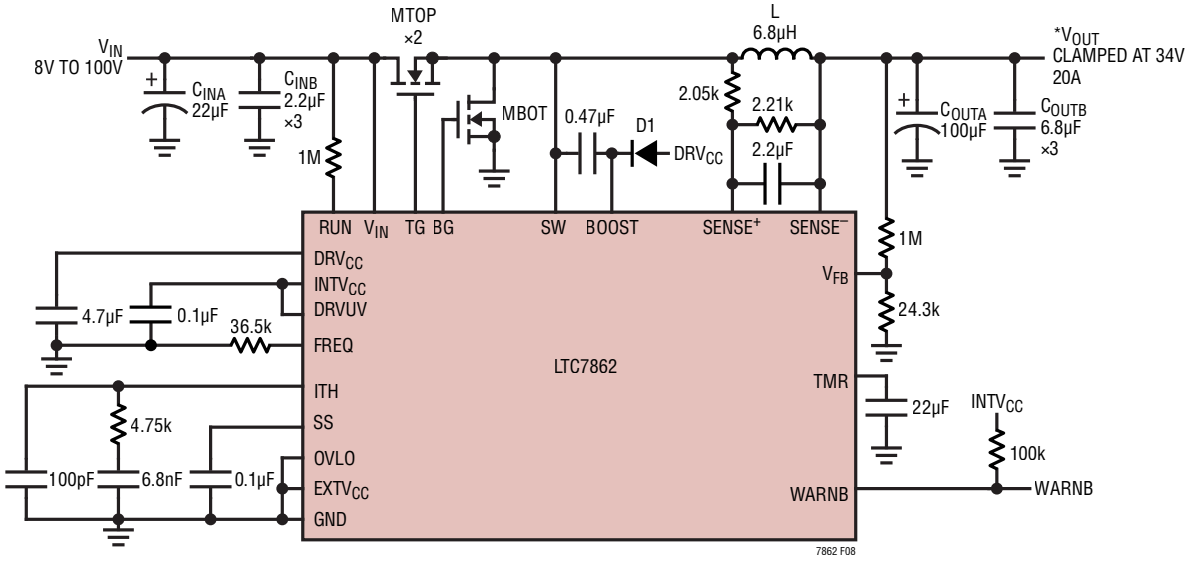
Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to

APPLICATIONS INFORMATION

the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top MOSFET and the bottom MOSFET to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS

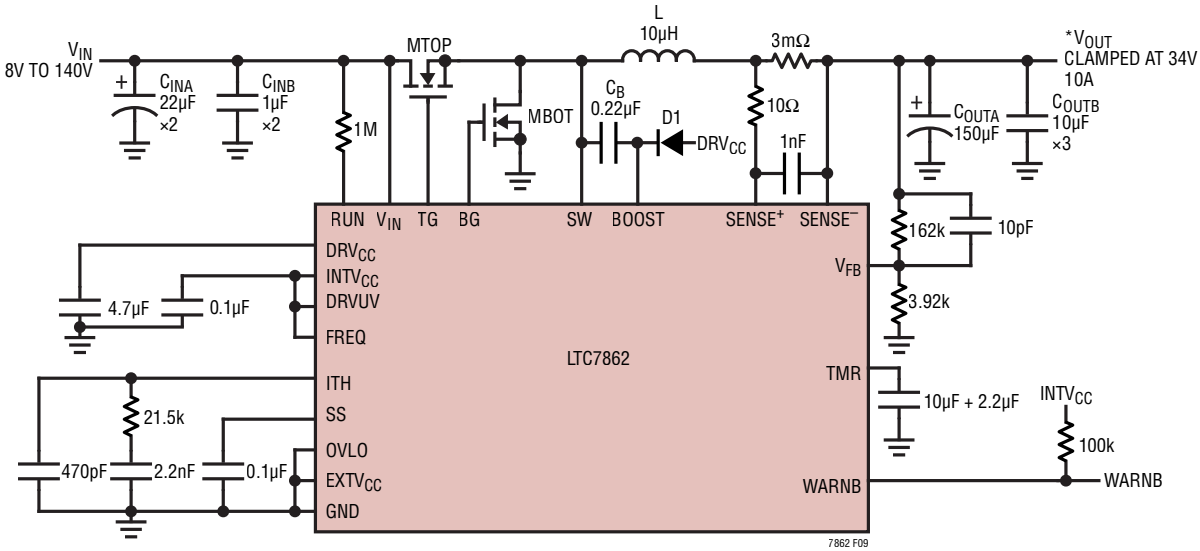


MTOP/MBOT: INFINEON BSC035N10NS5
L: COILCRAFT SER2918H-682KL
C_{INA}: SUNCON 160CE22LH
C_{INB}: TDK C4532X7R2A225K230KA

C_{OUTA}: SUN 63CE100LX
C_{OUTB}: TDK C4532X7R1H685K250KB
D1: NEXPERIA PNE20010ER

* V_{OUT} FOLLOWS V_{IN} WHEN V_{IN} < 34V
V_{OUT} CLAMPS AT 34V WHEN V_{IN} > 34V

Figure 8. 8V to 100V Input, 34V Maximum 20A Output at 200kHz



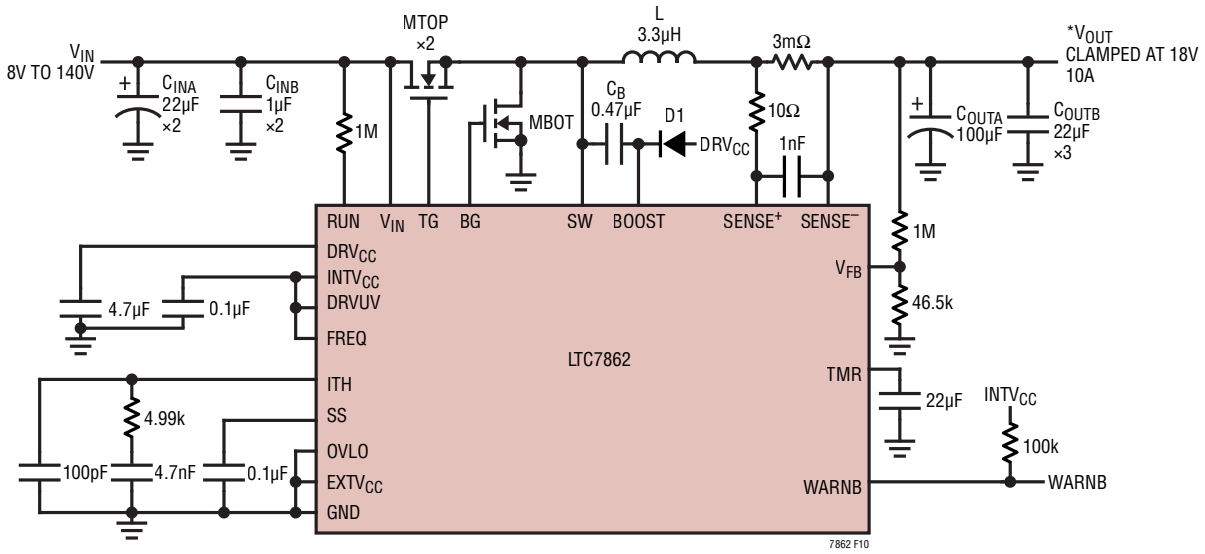
MTOP: BSC093N15NS5
MBOT: BSC160N15NS5
L: WURTH 74439370100
C_{INA}: NICHICON UVY2C220MPD1TD
C_{INB}: TDK CGA8P3X7T2E105M250KA

C_{OUTA}: SUNCON 50CE150AX
C_{OUTB}: MURATA GCM32EC71H106KA01L
CB: TDK CGA5L3X7T2E224K160AA
D1: NEXPERIA ES1DR

* V_{OUT} FOLLOWS V_{IN} WHEN V_{IN} < 28V
V_{OUT} CLAMPS AT 28V WHEN V_{IN} > 28V

Figure 9. 8V to 140V Input, 34V Maximum 10A Output at 535kHz

TYPICAL APPLICATIONS

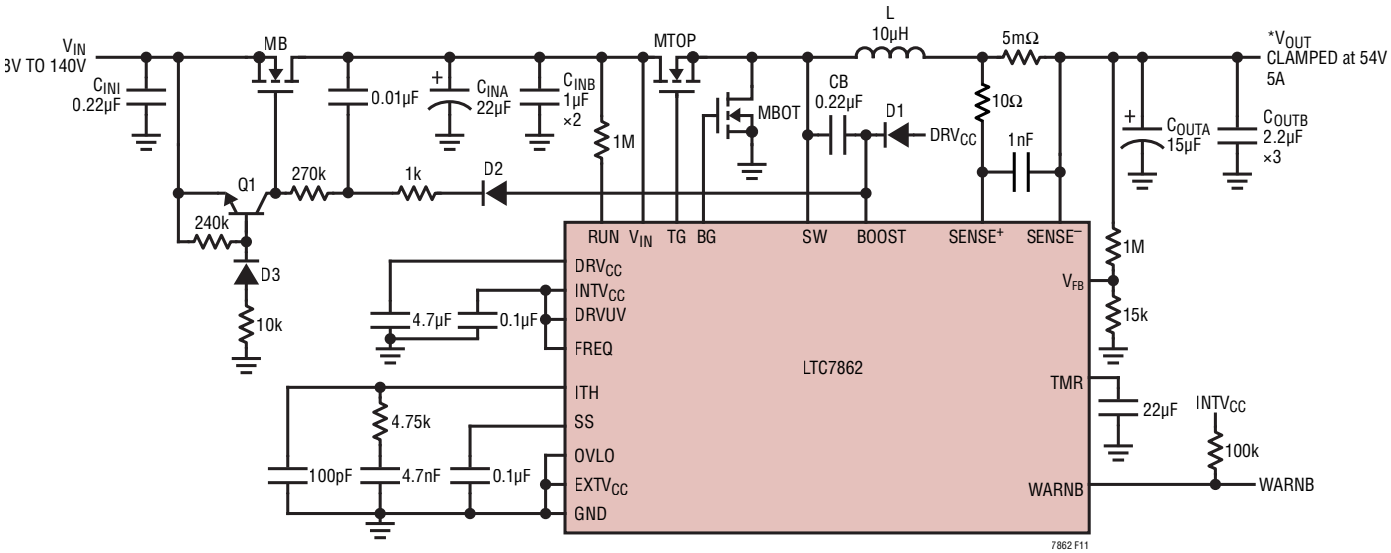


MTOP, MBOT: INFINEON BSC093N15NS5
L: COILCRAFT XAL1010-332ME
C_{INA}: SUNCON 160CE22LH
C_{INB}: TDK CGA8P3X7T2E105M250KA

C_{OUTA}: KEMET T521X107M025ATE060
C_{OUTB}: TDK C3225X5R1E226M250AC
CB: TDK CGA5L3X7T2E224K160AA
D1: NEXPERIA PNE20010ER

* V_{OUT} FOLLOWS V_{IN} WHEN V_{IN} < 18V
V_{OUT} CLAMPS AT 18V WHEN V_{IN} > 18V

Figure 10. 8V to 140V Input, 18V Maximum 10A Output at 535kHz



MB: INFINEON BSC093N15NS5
MTOP: INFINEON BSC093N15NS5
MBOT: INFINEON BSC160N15NS5
L: COILCRAFT XAL1010-103ME
C_{INI}: TDK C3225X7R2E224K200AA
C_{INA}: SUNCON 160CE47LHT
C_{INB}: TDK CGA8P3X7T2E105M250KA

C_{OUTA}: KEMET T521X156M063ATE035
C_{OUTB}: TDK C4532X7R2A225K230KA
Q1: ON SEMI MMBT3904
CB: TDK CGA5L3X7T2E224K160AA
D1: NEXPERIA PNE20010ER
D2, D3: CENTRAL SEMI CMDD3003

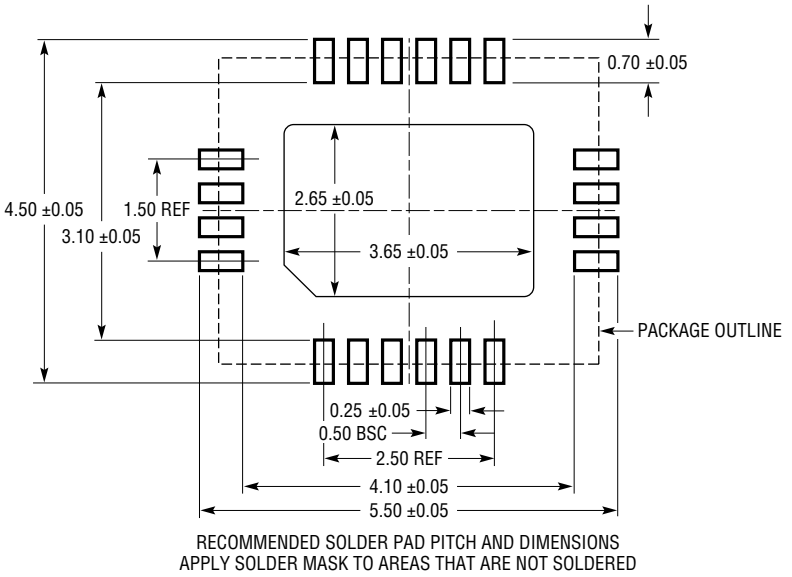
* V_{OUT} FOLLOWS V_{IN} WHEN V_{IN} < 54V
V_{OUT} CLAMPS AT 54V WHEN V_{IN} > 54V

Figure 11. 8V to 140V Input, 54V Maximum 5A Output at 535kHz with Reverse Input Protection

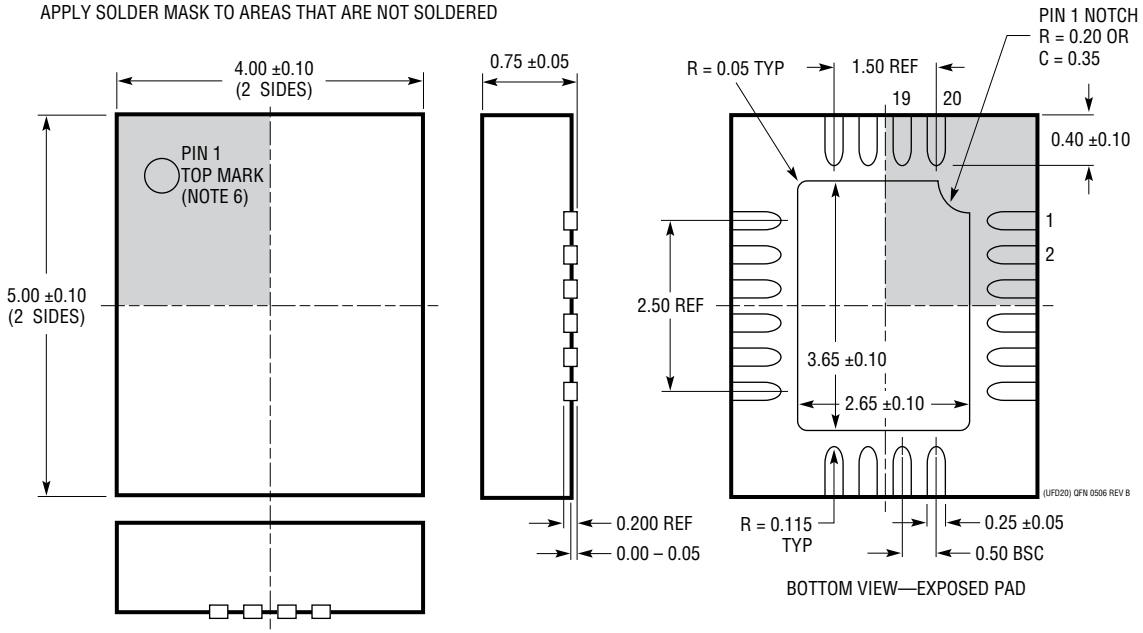
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC7862#packaging for the most recent package drawings.

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



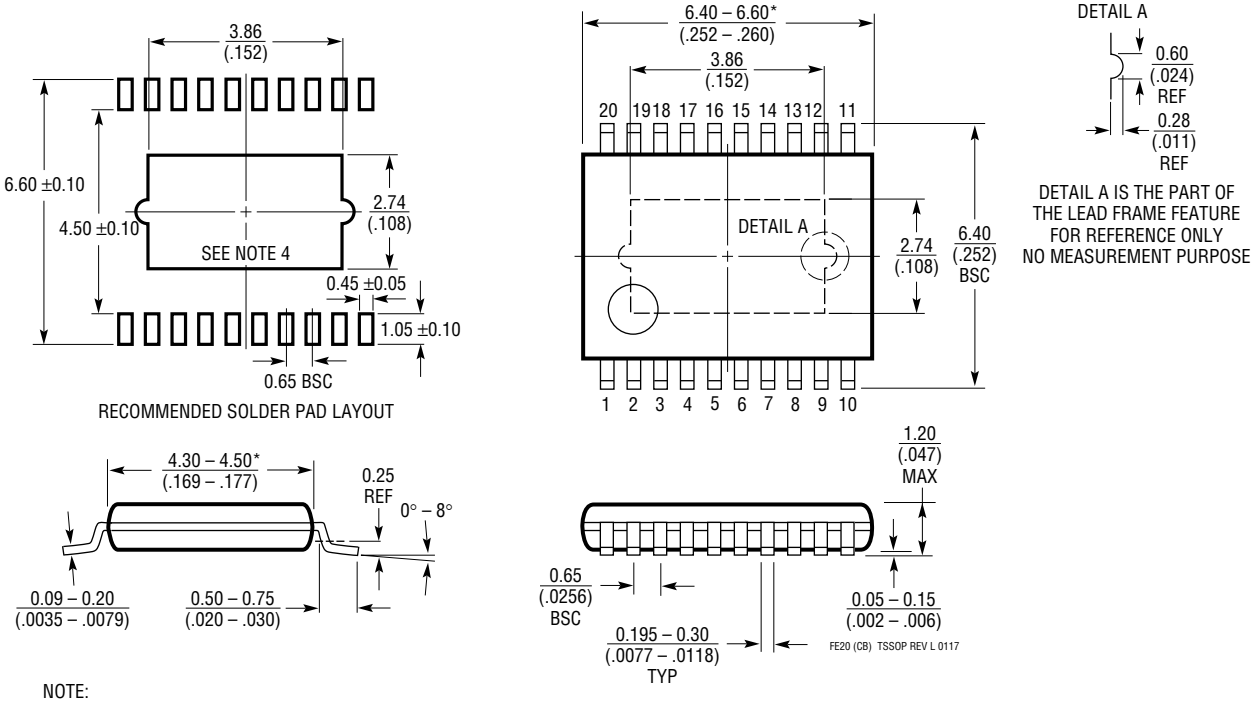
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC7862#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

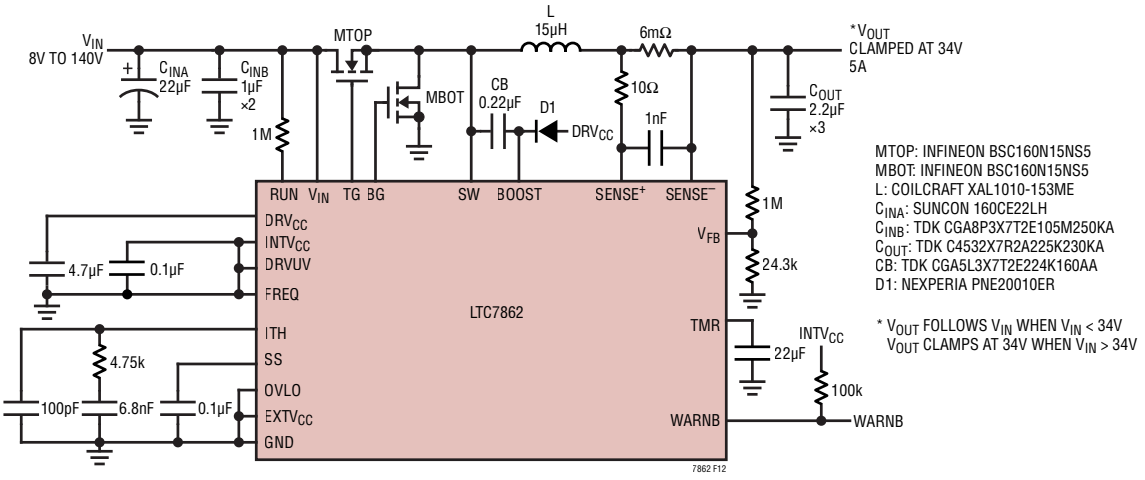


Figure 12. 8V to 140V Input, 5A 535kHz Surge Stopper for 24V or 28V Systems

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7860	High Efficiency Switching Surge Stopper	3.5V ≤ V_{IN} ≤ 60V, Expandable to 200V+, Adjustable V_{OUT} Clamp and Current Limit, Power Inductor Improves EMI, MSOP-12
LT4356	Surge Stopper with Current Limit	4V to 80V Operation; 100V Protection; DFN-12, MSOP-10 and SO-16 Packages
LTC4359	Ideal Diode Controller	4V to 80V Operation, –40V Input Protection, DFN-8 and MSOP-8 Packages
LTC4361	Overvoltage/Overcurrent Protection Controller	2.5V to 5.5V Operation, 80V Protection, TSOT-8 and DFN-8 Packages
LT4363	Surge Stopper with Current Limit	4V to 80V Operation; >100V Protection; DFN-12, MSOP-12 and SO-16 Packages
LTC4364	Surge Stopper with Ideal Diode	4V to 80V Operation; –40V to >100V Protection; DFN-14, MSOP-16 and SO-16 Packages
LTC4365	OV, UV and Reverse Input Protection Controller	2.5V to 34V Operation, –40V to 60V Protection, DFN-8 and TSOT-8 Packages
LTC4366	High Voltage Surge Stopper	9V to >500V Operation, Floating Topology, TSOT-8 and DFN-8 Packages
LTC4367	OV, UV and Reverse Input Protection Controller	2.5V to 60V Operation, –40V to 100V Protection, DFN-8 and MSOP-8 Packages
LTC4368	LTC4367 + Bidirectional Circuit Breaker	±50mV or +50mV/–3mV Circuit Breaker Thresholds; DFN-10, MSOP-10 Packages
LTC4380	Low Quiescent Current Surge Stopper	4V to 72V Operation, 80V Protection, 8µA, I_Q, MSOP-10, DFN-10 Packages
LTC3895/ LTC7801	150V Low I_Q, Synchronous Step-Down DC/DC Controller 100% Duty Cycle Capability, Adjustable 5V to 10V Gate Drive	4V ≤ V_{IN} ≤ 140V, 150V_{PK}, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 40µA PLL Fixed Frequency 50kHz to 900kHz
LTC3896	150V Low I_Q, Synchronous Inverting DC/DC Controller	4V ≤ V_{IN} ≤ 140V, 150V_{PK}, –60V ≤ V_{OUT} ≤ –0.8V, Ground-Reference Interface Pins, Adjustable 5V to 10V Gate Drive, I_Q = 40µA
LTC3871	Bidirectional PolyPhase® Synchronous Buck or Boost Controller	V_{HIGH} Up to 100V, V_{LOW} Up to 30V, High Power Buck or Boost On Demand
LTC3639	High Efficiency, 150V 100mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 150V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16 (12)
LTC3638	High Efficiency, 140V 250mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16 (12)
LTC7138	High Efficiency, 140V 400mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16 (12)
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2µA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN